

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

KOMURA et al.

Application No.: 09/921,561

Filed: August 6, 2001



Group Art Unit: 2816

Examiner: Minh T. Nguyen

Attorney Dkt. No.: 024016-00012

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For: DELAY CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CONTAINING
DELAY CIRCUIT AND DELAY METHOD

AMENDMENT AND FEE TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

Date: November 1, 2002

Sir:


Transmitted herewith is an Amendment in the above-identified patent application.

- ☐ A statement to establish small entity status under 37 C.F.R. §§1.9 and 1.27 is attached.
- ☐ Small entity status of this application under 37 C.F.R. §§1.9 and 1.27 has been established by a statement previously submitted.
- ☐ No additional claim fee is required.
- ☒ The claim fee has been calculated as shown below:

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE	OR	RATE	ADD'L FEE
TOTAL CLAIMS	31 MINUS	31	=0	x 9	\$		x 18	\$
INDEP CLAIMS	4 MINUS	3	=1	x 42	\$		x 84	\$84
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140	\$	OR	+280	\$
					\$			\$84

- ☒ Check number 349115 in the amount of \$194.00 is attached to cover the filing fees for a one-month extension of time and for adding one independent claim.

Respectfully submitted,


Rustan J. Hill
Registration No. 37,351

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810
RJH/mzk
TECH/145076.1



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Attorney Dkt. No.: 024016-00012

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CONTAINING A DELAY CIRCUIT AND DELAY METHOD

AMENDMENT UNDER 37CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

Date: November 1, 2002

Sir:

This paper is filed in response to the outstanding Office Action dated July 2, 2002, the time period for response having been extended until November 2, 2002 by the enclosed petition for extension of time. In the prosecution of the application identified above, please consider the following amendments.

IN THE CLAIMS:

Please cancel claim 3.

Please amend the claims as follows:

1. (Twice Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and
selecting switch sections, wherein

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